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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,410	10/22/2003	Theodore W. Houston	TI-34107.1	5967

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CT

Office Action Summary	Application No.	Applicant(s)	
	10/691,410	HOUSTON, THEODORE W.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 22 October 2003 and 03 January 2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 7-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 7-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the preliminary amendment filed on 10/22/03,

The examiner acknowledges claims 1-6 and 14-20 have been canceled and claims 7-13 are pending.

Specification

In the first page of the specification, "This is a division of Application No. 10/233,352, filed 08/30/2002" should be changed/updated to - - This is a division of Application No. 10/233,352, filed 08/30/2002 and now US Patent 6,734,521 - -.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a), which forms the basis for all obviousness rejections, set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 7-12 are rejected under 35 U.S.C. 102(e) as being anticipated by, or in the alternative, under 35 U.S.C. 103(a) as obvious over US 6,369,412 to Ueda et al.

(Claim 7)

providing a first transistor a first logic path (fig 1, 4-10), the first transistor having a first contact, a first gate length and a first contact to gate centerline spacing (fig 1(a));

providing a second transistor in a second logic path (fig 1, 4-10), the second transistor having a second contact, a second gate length and a second contact to gate centerline spacing (fig 1(b)), the first contact to gate centerline spacing substantially equal to the second contact to gate centerline spacing (this limitation is considered taught by, or obvious over Ueda et al., especially given the breadth of the term

"substantially." In figures la and b for example, Ueda et al. assign identical reference numerals 13-15 to designate P-type source/drain regions (col. 9, lines 8-9) over which gates having different lengths traverse. Because the source/drain regions are identified the same, it is considered inherent that they posses the same parameters such as doping as well as size. Ueda et al. also show in figures 7 and 8 the wiring layers formed to make contact to the source/drain regions 13-15. As shown, the contacts are centered in regions 13-15. As such, the contact to gate centerline spacing would be the same.

It is also considered obvious that Ueda et al. would form the contact to gate centerline spacing substantially the same. In figure 9, Ueda et al. teach, in one cell area 2, formation of both first and second gate lengths L1 and L2. It is considered obvious in the design of semiconductor devices that similar wells (e.g. N-type wells 16-18 and 47-49) would be formed having the same dimensions to reduce processing variables. This is especially true in figure 9 where the same polarity wells are formed in the same chip area 2. As shown in figure 10, Ueda et al. form contacts to the N-type regions which are centered over these regions such that the contact to gate centerline spacing would be the same); and

selecting a different gate length for the first gate length using a predetermined design criterion (abstract, background, summary, col 10, 12).

(Claim 8) wherein the first gate length and the second gate length are equal, and selecting a different gate length comprises selecting a different gate length without changing the placement the first contact or the second contact (fig 1, 6-10).

(Claim 9) wherein providing a first transistor comprises providing a first cell comprising the first transistor and wherein selecting a different gate length comprises replacing the first cell with a substitute cell comprising a substitute transistor, the substitute transistor having a different gate length than the first gate length (abstract, background, summary, col 10), the first cell and the substitute cell having the same footprint (fig 1(a) and fig 1(b)) and operable to perform a same function.

(Claim 10) wherein the predetermined design criterion is based on the respective levels of leakage current of the first transistor and the second transistor (col 1 line 67 to col 2 line 1, col 12 line 27).

(Claim 11) wherein the first logic path is a critical path (critical or not critical are a relative terms, logic paths in this prior art are considered critical or non-critical accordingly) and the different gate length is a gate length that is shorter than the first gate length (abstract, background, summary).

(Claim 12) wherein the first logic path is a non-critical path (critical or not critical are a relative terms, logic paths in this prior art are considered critical or non-critical accordingly) and the different gate length is a gate length that is longer than the first gate length (abstract, background, summary).

2. Claims 7-9, 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Gardner et al. (USP 6453447)

(Claim 7)

providing a first transistor a first logic path, the first transistor having a first contact, a first gate length and a first contact to gate centerline spacing (fig 1-7, 10);

providing a second transistor in a second logic path, the second transistor having a second contact, a second gate length and a second contact to gate centerline spacing (fig 1-7, 10), the first contact to gate centerline spacing substantially equal to the second contact to gate centerline spacing (fig 3-5, 10, col 10 line 60+); and

selecting a different gate length for the first gate length using a predetermined design criterion (fig 1-10).

(Claim 8) wherein the first gate length and the second gate length are equal, and selecting a different gate length comprises selecting a different gate length without changing the placement the first contact or the second contact (fig 3-5, 7, 9).

(Claim 9) wherein providing a first transistor comprises providing a first cell comprising the first transistor and wherein selecting a different gate length comprises replacing the first cell with a substitute cell comprising a substitute transistor, the substitute transistor having a different gate length than the first gate length (fig 1-10), the first cell and the substitute cell having the same footprint (fig 5, 10, col 5 line 3+) and operable to perform a same function.

(Claim 11) wherein the first logic path is a critical path (critical or not critical are a relative terms, logic paths in this prior art are considered critical or non-critical accordingly) and the different gate length is a gate length that is shorter than the first gate length (fig 2-10).

(Claim 12) wherein the first logic path is a non-critical path (critical or not critical are a relative terms, logic paths in this prior art are considered critical or non-critical accordingly) and the different gate length is a gate length that is longer than the first gate length (fig 2-10).

(Claim 13) wherein modeling a change of the gate length comprises changing the gate length by a length increment, the length increment less than the length of one grid of a design rule for the IC (col 7).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Patent Examiner

Paul Dinh
2/9/05